HA-2850 SPICE Operational Amplifier Macro-Model

Introduction

This application note describes the SPICE macro-model for the HA-2850, a wide bandwidth op amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the SPICE net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model is designed to emulate a typical rather than a worst case part. Most AC and DC parameters are simulated. Significant poles and zeros are included to give the most accurate AC and transient simulation with minimum complexity.

Model Description

Input Stage

D_P and D_N represent the differential input resistance. Input bias currents are created by I_1 and offset current is modeled with F_A. Source V_N represents the input offset voltage. No input parasitics due to package capacitance and lead inductance are included.

Gain Stage

G_2, R_2, C_C, G_{OL}, and R_D simulate open loop gain. C_C is the macro-model dominant pole capacitor, which effects slew rate and bandwidth.

Poles and Zeros

The HA-2850 macro-model uses a combination of complex zeros modeled with an RLC network plus a pole-zero pair and three additional poles using RC networks.

Output Stage

E_{X1}, D_1 and D_2 model output current limiting. I_H and I_L are the power supply currents. D_{PH}, D_{PL} and G_{PS} vary the supply currents based on the op amp's output current. D_L, D_H, E_{CC} and E_{EE} provide voltage clamping on the output to simulate the typical output voltage swing. Some effects of output parasitics due to package capacitance and inductance are lumped with the poles.

Parameters Not Modeled

To maintain a simple macro-model, not all op amp parameters are modeled. Most of the parameters not modeled are listed below:

- Temperature Effects
- Differential Voltage Restrictions
- Input Voltage and Current Noise
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Power Supply Range

Spice Listing

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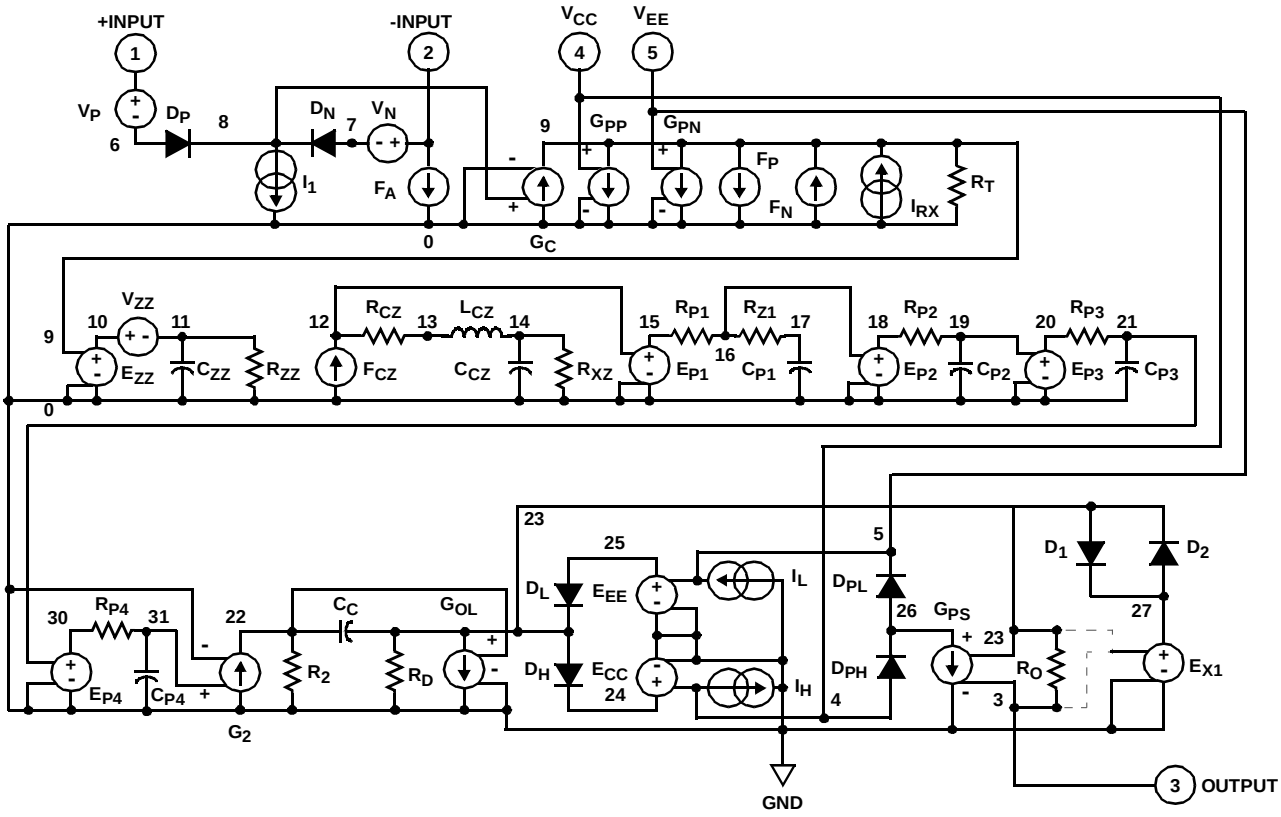
*
*  HA-2850 MacroModel
*  Rev: 06-10-98 Alan Erzinger and Jeff Lies
*
*  Pinout:  +In -In Vcc Vee Out
*
.SUBCKT HA2850 1 2 4 5 3
.MODEL DP D  IS=+1.0E-17  N=+2.3872
.MODEL DN D  IS=+1.0E-17    N=+2.3872
.MODEL DV D  IS=+1.6146E-13  N=.2
.MODEL D1 D  IS=1E-9  N=1
.MODEL D2 D  IS=1E-9  N=+1.0
.MODEL DX D  IS=1E-20  N=+30.0
*
*      Input Stage
*  Value of source VN models VIO and may be
adjusted as desired.
*
VP 1 6 0
VN 2 7 +1.0E-03
I1 8 0 +1.004E-05
FA 2 0 VN +2.156998E-01
DP 6 8 DP
DN 7 8 DN
FP 9 0 VP  +6.03E+02
FN 0 9 VN  +6.029E+02
GC 0 9 8 0 +2.7311E-06
GPP 9 0 4 0 +3.4326E-06
GPN 9 0 5 0 +3.8529E-06
IRX 0 9 -3.0927E-06
RT 9 0 1.0
*
*      Poles and Zeros
EZZ 10 0 9 0 1.0
VZZ 10 11 0.0
CZZ 11 0 1E-12
RZZ 11 0 1E+07
FCZ 0 12 VZZ  1.0
RCZ 12 13 +1.7407E+01
LCZ 13 14 +6.1841E-08
CCZ 14 0 1E-12
RXZ 14 0 1E+07
EP1 15 0 12 0 1.0
RP1 15 16 +7.2967
RZ1 16 17 +1.99
CP1 17 0 1E-10
EP2 18 0 16 0 1.0
RP2 18 19 +4.5486
CP2 19 0 1E-10
EP3 20 0 19 0 1.0
RP3 20 21 +8.0
CP3 21 0 1E-10
EP4 30 0 21 0 1.0
RP4 30 31 +8.0
CP4 31 0 1E-10
*
*      Output Stage
G2 0 22 31 0 1.0
R2 22 0 +5.0577E+02
CC 22 23 +1.590E-11
GOL 23 0 22 0 +2.0104E+03
RD 23 0 +6.07E-01
DH 23 24 DV
DL 25 23 DV
ECC 24 0 POLY 1  4 0 -2.4167  1.0
EEE 25 0 POLY 1  5 0 +2.5203  1.0
IH 4 0 +7.5422E-03
IL 0 5 +7.5382E-03
GPS 26 0 23 3 +2.6302E-02
DPH 4 26 DX
DPL 26 5 DX
D1 23 27 D1
D2 27 23 D2
EX1 27 0 POLY 2  23 0 3 0 0.0   +7.8568E-01
+2.1269E-01
RO 23 3 +3.80195E+01
.ENDS HA2850
```

Macro-Model Schematic



Model Performance

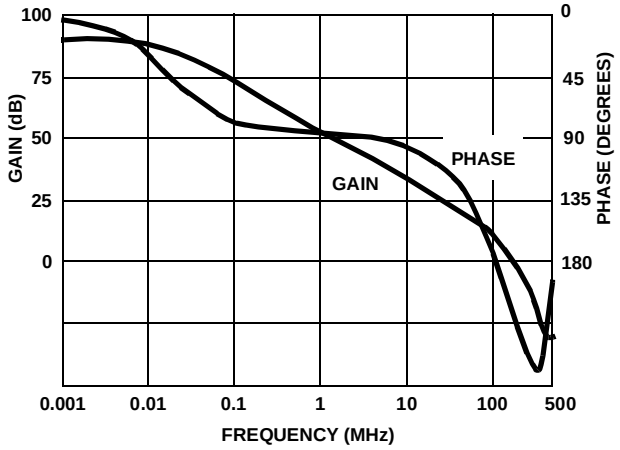


FIGURE 1. GAIN/PHASE RESPONSE vs FREQUENCY

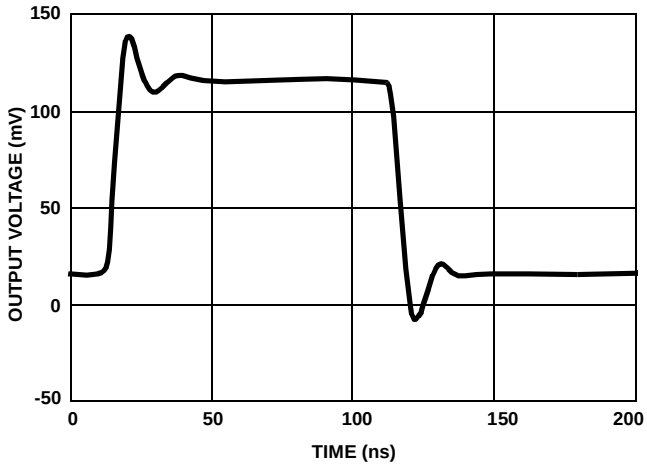


FIGURE 2. SMALL SIGNAL RESPONSE

Model Performance (Continued)

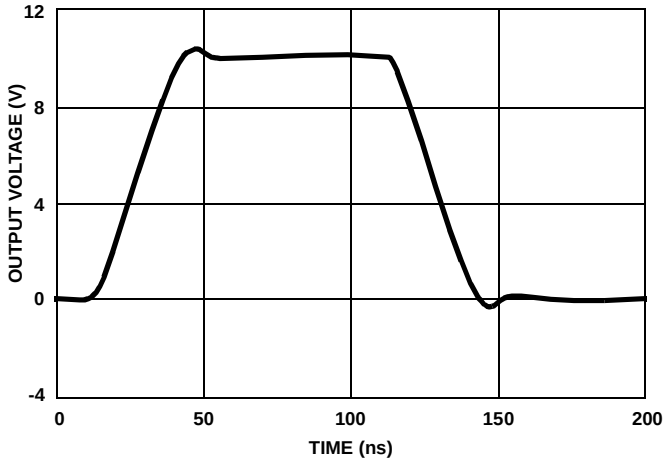


FIGURE 3. LARGE SIGNAL RESPONSE

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